

# **ESD** Protection

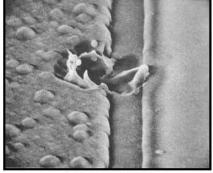
Kenneth Toomey Field Application Engineer AEM Electronics (USA), Inc.

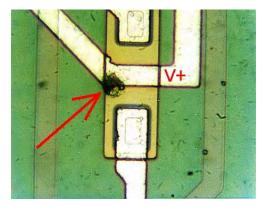
ktoomey@aemcomponents.com

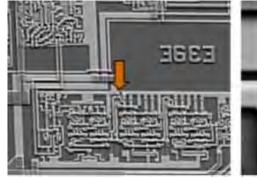


# Effect ESD has on IC's?

- Electrostatic Discharge is the transfer of static charge between two objects of different potential that come in to contact
- Can generate between 1,500V to 35,000V
- Leading cause of device failure







Surface damage at 4300X





# **New ESD Challenges**

- IC nanometer technology is more vulnerable to ESD
- High speed interfaces and data ports
  - USB 3.0 5Gbit/sec
  - HDMI 1.3 3.4Gbit/sec
  - IEEE 1394 400/800/3200Mbit/sec



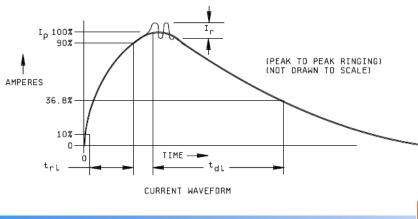


## **ESD Standards**

#### MIL-STD-883, Method 3015

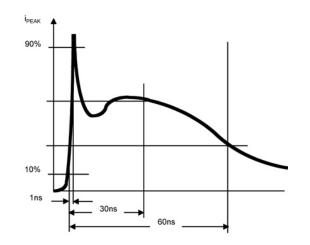
- Required for "on-chip" ESD protection during chip manufacturing
- Also known as the "Human Body Model" (HBM)
- Discharges a 100pF capacitor into a 1500Ω resistor
- HBM Level 4: Peak Current 2.67A at 4kV
- Rise time: 10ns

**Confidential** 



#### IEC61000-4-2

- Required by equipment manufacturers for system or application level testing
- Discharge a 150pF into a 330Ω resistor
- IEC Level 4: Peak Current 30A at 8kV
- Rise Time: 1ns





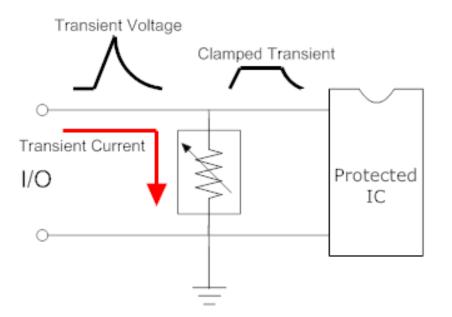
# **ESD Standards Comparison**

Level	HBM		IEC	
	Contact Discharge (kV)	Peak Current (A)	Contact Discharge (kV)	Peak Current (A)
1	0.5	0.33	2	7.5
2	1	0.67	4	15
3	2	1.33	6	22.5
4	4	2.67	8	30



## **ESD** Protection

- Non-linear voltagecurrent characteristic
  - Low voltage high resistance
  - High voltage low resistance
- Provides low impedance shunt path to ground





# **Design Considerations**

- Capacitance and signal integrity
- Max ESD withstanding capability of protected device
- Min ESD shot withstanding cycle of ESD device
- Package size and PCB layout

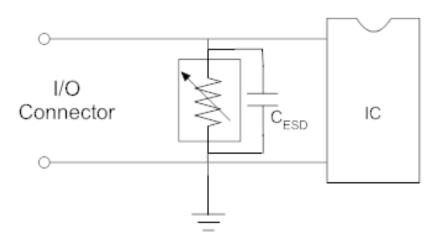
- Clamping Voltage
- Breakdown/Trigger voltage





## Capacitance and Signal Integrity

- All ESD device have some level intrinsic capacitance
- Parallel capacitance attenuates high frequency signals
- High capacitance causes signal degradation as signal frequencies increase

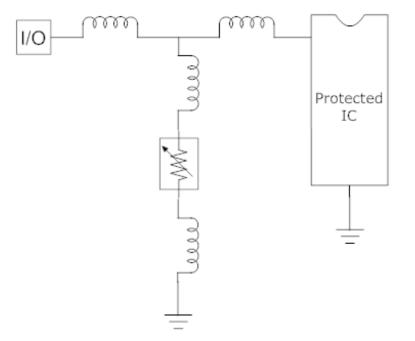




### **Board Layout**

- Place ESD device as close as possible to I/O port or source of ESD entry
- Reduce trace length to minimize parasitic inductance
- Parasitic inductance can cause a large voltage spike and increase clamping voltage through the relationship:

$$\mathbf{V} = \mathbf{L} \frac{di}{dt}$$



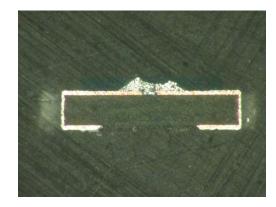
ex. A trace that measures just 2nH will produce a 60V spike for an 8kV ESD strike.

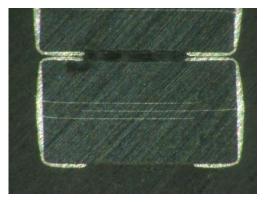
$$L\frac{di}{dt} = 2$$
nH  $\left(\frac{30}{1ns}\right) = 60$ V



# **Types of ESD Devices**

- Polymer Based
  - Pros:
    - Ultra low cap 0.05pF to 0.5pF
    - Low cost
  - Cons:
    - High trigger and clamping voltage
    - Low ESD strike withstanding capability
- Low Cap MLV
  - Pros:
    - Low cap 0.1 to 1pF through sorting
    - Low cost
  - Cons:
    - High clamping voltage
    - High leakage current
    - Low ESD strike withstanding capability

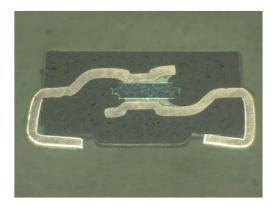






# **Types of ESD Devices**

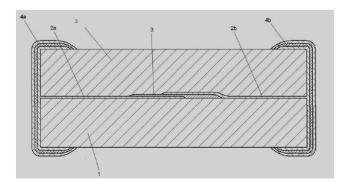
- TVS Diode
  - Pros:
    - High ESD strike
      withstanding capability
  - Cons:
    - High cost





### AEM GcDiode<sup>TM</sup>

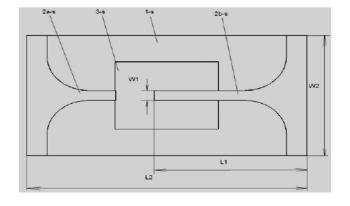
The GcDiode is based on a glassceramic dual phase material system with proprietary ESD functional material that provides non-linear resistance at different voltage conditions



#### Key Features

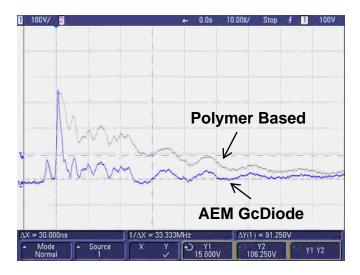
- Low clamping voltage (30V)
- Low capacitance (0.25pF)
- Low leakage current (0.1nA)
- Fast response time (1ns)
- High ESD shot withstanding capability
- Bi-Directional

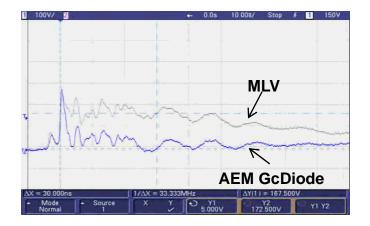


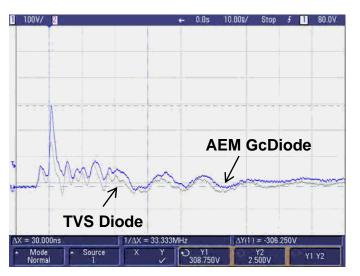




# **Comparison ESD Suppression**





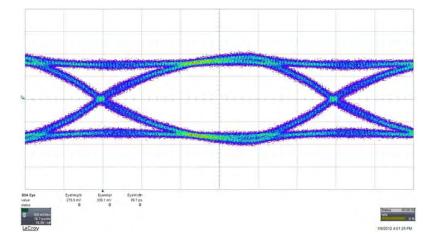


- Typical IEC61000-4-2 level 4 contact discharge (8kV) suppressed waveform.
- GcDiode has similar performance
  as the TVS Diode

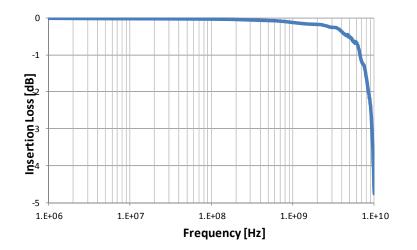


### GcDiode<sup>™</sup> Signal Integrity 10Gbit/sec

#### Eye Diagram

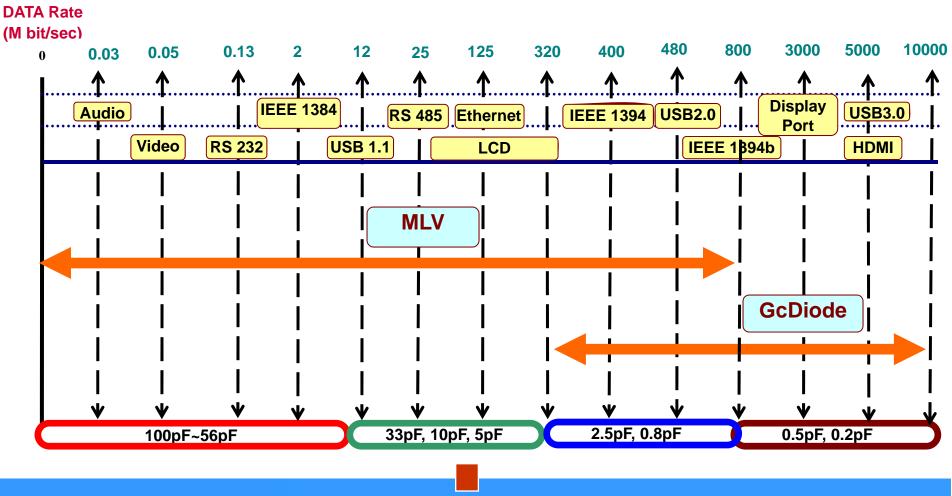


#### **Insertion Loss (S21)**





### **ESD Selection**





## Conclusion

- The main purpose of "On-Chip" ESD protection is to protect the IC against an ESD event during the manufacturing environment of the IC
- Supplementary ESD protection is required for system level/application ESD events
- Low capacitance to maintain signal integrity for high speed data ports
- Minimize parasitic inductance to maximize performance of ESD device
- GcDiode<sup>™</sup> is similar in performance to the TVS Diode